

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. **(Currently Amended)** A method for transferring a first root key between a key provider system and a second other system via an information network comprising the steps of:
 - a) encrypting the first root key using a first super-root key of the key provider system;
 - b) providing within the second other system a first secure module having a second super-root key within a read-only memory circuit thereof and provided with the first secure module, the second super-root key accessible only by program code being executed on a processor internal to the first secure module, and wherein the second super-root key is other than modifiable and other than accessible outside of the module, and wherein the second super-root key is a private key;
 - b1) automatically generating by the first secure module a root key request in dependence on a root key status;
 - c) transferring the encrypted first root key from the key provider system to the second other system via the information network in response to the root key request;
 - d) providing the encrypted first root key to the processor internal to the first secure module of the second other system; and,
 - e) executing program code on the processor internal to the first secure module to decrypt the encrypted first root key using the second super-root key stored within the read-only

memory circuit of the first secure module and to store the decrypted first root key internally within a secure key memory location of the first secure module;

wherein the second super-root key and the first super-root key are the private and public portions of an asymmetric private/public-key pair, respectively.

2. (Previously Presented) The method according to claim 1 wherein the processor internal to the module accesses the second super-root key only for decrypting encrypted root keys, wherein the decrypted root keys are then stored within the module inaccessible outside the secure module.

3. (Original) The method according to claim 2 wherein the step (a) is performed in a corresponding secure module.

4. (Previously Presented) The method according to claim 3 wherein the processor internal to the first secure module accesses the second super-root key only in response to a request from the corresponding secure module.

5-6. **Canceled.**

7. **(Currently Amended)** The method according to ~~claim 6~~ claim 1 comprising the additional step prior to step a) of: a1) generating a first root key within a key-generating processor internal to the key provider system.

8. (Original) The method according to claim 7 wherein the key-generating processor is embodied on the corresponding secure module.

9. Canceled.

10. (Previously Presented) A method for transferring a first super-root key between a key provider system and a second other system via an information network comprising the steps of:

a) encrypting the first super root key using a second super-root key of the key provider system;

b) providing within the second other system a first secure module having third and fourth super-root keys within a memory circuit thereof, the third and fourth super-root keys accessible only by program code being executed on a processor internal to the first secure module for decrypting encrypted root keys and encrypted super-root keys and for storing the decrypted keys within a memory circuit of the first secure module, and wherein the third and fourth super-root keys are other than accessible outside of the module, and wherein the third and fourth super-root keys are private keys;

b1) automatically generating by the first secure module a super-root key request in dependence on a super-root key status;

c) transferring the encrypted first super-root key from the key provider system to the second other system via the information network in response to the super-root key request;

d) providing the encrypted fourth super-root key to the processor internal to the first secure module of the second other system; and,

e) executing program code on the processor internal to the first secure module to decrypt the encrypted first super-root key using the third super-root key stored within the memory circuit of the first secure module and to store the decrypted first super-root key internally within a secure key memory location of the first secure module.

11. (Previously Presented) A method for transferring a first super-root key between a key provider system and a second other system via an information network according to claim 10 further comprising the steps of:

f) executing program code on the processor internal to the first secure module to store the decrypted first super-root key within the memory circuit of the first secure module at a location corresponding approximately to the location where the fourth super-root key was stored.

12. (Previously Presented) The method according to claim 11 wherein one of the third and fourth super-root keys are only replaceable through use of the other of the third and fourth super-root keys.

13. Canceled

14. (Previously Presented) The method according to claim 11 wherein the step of storing the decrypted first super-root key comprises the steps of:

i1) erasing the fourth super-root key from a first storage area of the memory circuit;
and,

i2) storing the decrypted first super-root key within approximately the same first storage area of the same memory circuit.

15. **(Currently Amended)** A secure module for use in a system for transferring a secure root key between a key provider system and a second other system via an information network that is other than secure, the secure module in operative communication with the second other system, the secure module including:

an encryption processor;

an input port for receiving encrypted electronic data from outside the module and for providing the encrypted electronic data to the encryption processor;

a memory circuit in operative communication with the encryption processor for storing at least a first super-root key;

memory storage having program code stored therein and executable on the encryption processor for, upon receipt of an encrypted secure root key, decrypting the encrypted secure root key using the at least a first super-root key and for storing the decrypted secure root key within the memory circuit, the at least a first super-root key being other than accessible by any code other than the program code and being other than modifiable thereby, wherein the at least a first super-root key is a private key of a private/public-key pair; and

a root key request generator for generating a root key request in dependence on a root key status.

16. (Previously Presented) The secure module according to claim 15 wherein the code executable on the encryption processor accesses the at least a first super-root key only in response to a request from a corresponding secure module.

17. (Previously Presented) The secure module according to claim 16 wherein the code executable on the encryption processor is for performing encryption functions the results of which are inaccessible outside of the module.

18. (Previously Presented) The secure module according to claim 17 wherein the memory circuit for storing the at least a first super-root key is a read-only memory circuit.

19. (Previously Presented) The secure module according to claim 18 wherein the module is FIPS 140 compliant.

20. (Previously Presented) The secure module according to claim 19 wherein the module includes a tamper detection circuit for erasing the at least a first super-root key in dependence upon a detected attempt to access the electronic contents of the module in an unauthorized fashion.

21. (Previously Presented) A secure module for use in a system for transferring a secure super-root key between a key provider system and a second other system via an information network that is other than secure, the secure module in operative communication with the second other system, the secure module including:

an encryption processor;

an input port for receiving encrypted electronic data from outside the module and for providing the encrypted electronic data to the encryption processor;

a memory circuit in operative communication with the encryption processor for storing a first super-root key within a first memory location thereof and for storing a second super-root key within a second other memory location thereof;

memory storage having program code stored therein and executable on the encryption processor for, upon receipt of an encrypted third super-root key, decrypting the encrypted third super-root key using one of the first and second super-root keys and for storing the decrypted third super-root key at a memory location corresponding to the other one of the first and second super-root keys, the first, second, and third super-root keys when stored in the memory circuit being accessible only by the program code and being modifiable only by the program code for all modifications excluding erasure, wherein the first, second, and third super-root keys are private keys; and

a super-root key request generator for generating a super-root key request in dependence on a super-root key status.

22. (Previously Presented) The secure module according to claim 21 wherein the code executable on the encryption processor accesses the super-root keys stored in the memory circuit only in response to a request from a corresponding secure module.

23. (Previously Presented) The secure module according to claim 22 wherein the code executable on the encryption processor is for performing encryption functions the results of which are inaccessible outside of the module.

24. (Previously Presented) The secure module according to claim 23 wherein the memory circuit for storing the super-root keys is a non-volatile reprogrammable memory circuit.

25. (Previously Presented) The secure module according to claim 23 wherein the memory circuit for storing the super-root keys is one of an electrically erasable programmable read-only memory (EEPROM) circuit and a random access memory (RAM) circuit having an on-board power supply in the form of a battery.

26. (Previously Presented) The secure module according to claim 25 wherein the module is FPS140 compliant.

27. (Previously Presented) The secure module according to claim 26 wherein the module includes a tamper detection circuit for erasing every cryptographic key stored within the memory circuit in dependence upon a detected attempt to access the electronic contents of the module in an unauthorized fashion.

28-31. Canceled

32. (Previously Presented) The method of claim 1 wherein the first root key is for at least one of encrypting and decrypting key pairs that are used for encrypting and decrypting messages between the second other system and one or more client stations.

33. (Previously Presented) The method of claim 10 wherein the first, third, and fourth super-root keys are only for decrypting at least one of encrypted private root keys and encrypted private super-root keys generated by the key provider system.